


I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

**PATENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
On 4/15/03

TOWNSEND and TOWNSEND and CREW LLP

By 

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

**Maria C. Y. Quinones, et al.**

Application No.: 09/487,969

Filed: January 18, 2000

For: **IMPROVED METHOD OF  
MAKING A CHIP DEVICE**

Examiner: **Alonzo Chambliss**

Art Unit: **2814**

**DECLARATION UNDER  
37 C.F.R. § 1.131**

Sir:

We, **Maria Clemens Y. Quinones, Gilmore S. Baje, Maria Cristina B. Estacio, Marvin R. Gestole, Oliver M. Ledon, and Santos Mepieza**, each declare as follows:

1. I am a co-inventor of at least one claim in the referenced patent application.
2. I have reviewed the Office Action mailed on December 31, 2002, and the obviousness rejections of claims 7-33 based on U.S. Patent No. 6,307,755 to Williams et al.
3. The inventions of at least pending independent claims 7, 15, and 23 were conceived of before May 27, 1999, the filing date of Williams et al. Evidence of conception is shown by the attached documents in Exhibit A. Some of the pages in Exhibit A include initials and dates of January 5 and 6, 1999.

Maria C. Estacio, et al.  
Application No.: 09/548,946  
Page 2

PATENT

4. Reduction to practice of embodiments of the inventions before May 27, 1999, is evidenced by the documents in Exhibits B and C, which include e-mail communications between one or more co-inventors and others. A die package that was produced according to an embodiment of the invention was referred to internally at Fairchild Semiconductor as "SO-8" wireless. As evidence of reduction to practice, one e-mail communication in Exhibit B states "Wireless samples (SO-8) were sent from Steve Sapp with objective of identifying source of Rdson lower than expected." One e-mail in Exhibit C states "Add top & bottom alignment press-fit studs & holes ... Status: Changes incorporated in Rev. P bottom frame and Rev. N topframe design." The documents in Exhibits B and C were originally created before May 27, 1999 and show that an embodiment of the invention was reduced to practice before May 27, 1999.
5. Exhibit D contains correspondence regarding the preparation of a patent application for embodiments of the invention. The correspondence includes: a letter dated June 4, 1999 from Fairchild Semiconductor to Townsend, Townsend & Crew (TTC) requesting the preparation of a patent application; a letter dated June 7, 1999 from TTC acknowledging receipt of the June 4, 1999 letter; a file note dated September 20, 1999 with some invention details; a letter dated November 19, 1999 from TTC to Ms. Quinones with a draft patent application; and an e-mail dated December 5, 1999 with comments on the prior draft patent application.
6. As shown by Exhibits A-C, I believe that an embodiment of the invention was conceived of and reduced to practice before May 27, 1999. As shown by Exhibits A-D, embodiments of the invention were also conceived of before May 27, 1999 and were diligently pursued until the filing of the present application.

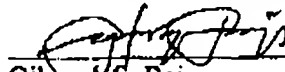
Maria C. Estacio, et al  
Application No.: 09/548,946  
Page 3

PATENT

7. The acts relied on in this Declaration (and described in the Exhibits) took place in a WTO country
8. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. §1001) and may jeopardize the validity of the application or any patent issuing thereon.

  
Maria Clemens Y. Quiñones


Date

  
Gilmore S. Baje


Date

  
Maria Cristina B. Estacio

Date

  
Marvin R. Gestole

Date

  
Oliver M. Ledon

Date

  
Santos Mepieza

Date

0002224 v.1